

Analysis and Processing of Power Output Signal of 200V Power Devices

Cheng-Yen Wu¹, Hsin-Chiang You^{*2}, Chen-Chung Liu³, Wen-Luh Yang⁴

¹Ph.D. Program of Electrical and Communications Engineering, Feng Chia University/No. 100, Wenhwa Rd., Taichung 40724, Taiwan (R.O.C.)

^{*2,3}Department of Electronic Engineering, National Chin-Yi University of Technology/No.57, Sec. 2, Zhongshan Rd., Taiping Dist., Taichung 41170, Taiwan (R.O.C.)

⁴Department of Electronic Engineering, Feng Chia University/No. 100, Wenhwa Rd., Taichung 40724, Taiwan (R.O.C.)

¹yenwu@ncut.edu.tw; ^{*2}hcyou@ncut.edu.tw; ³ccl@ncut.edu.tw; ⁴wlyang@fcu.edu.tw

Abstract

In the development of semiconductors, power devices have more and more applications. In addition to today's popular PC and smartphone. LED energy-saving development must rely on the power devices. In this study, the design direction is focused on 200 V power devices. In addition, this device can be used in consumer electronics products, and it will be the next focused design points to be improved. The same production process technology is applied on fabricating the devices in the silicon substrate and the SOI substrate to explore the difference between both devices in the electric potential, electric field, the depletion region and breakdown voltage.

Keywords

200 V; SOI; Breakdown Voltage; Power Devices

Introduction

In this technologically advanced generation, the development of computers is increasing. From early 286 computers to the current Intel core i7, the effectiveness of the computer is increasing. In general, on a computer motherboard, there are a well-known CPU, memories, sound chips, display chips and other devices. However, the motherboard possesses very important devices used in the board with the total count of 5 ~ 10. This device is Power MOSFET (Power Metal Oxide Semiconductor Field Effect Transistor) [1-3]. Currently, power devices have been applied in a variety of electrical appliances, and play an important role in the electrical products.

Since the main application of power devices is used for driving and protecting circuits. The power devices are inevitably heated during the operation. In these circumstances, the development of the structure of the power devices are derived from the traditional DMOS structure, slowly extended to VMOS, UMOS, IGBT and then developed into COOLMOS LDMOS, etc. [4-7]. In addition, the heating problem of power devices must also be avoided due to high on-resistance of the power device, and whether the remanded power can be reached. Today in LDMOS process technology, academic units are exploring the ability to withstand the power. However, to explore some of the voltage- withstanding techniques are designed to achieve the production of high-voltage power devices. In the current generation of computers popularly used, the development of computers has changed from desktops to laptops, and today is more focused on tablet PC development. Tablet devices technology integrated with mobile communications, is now used to have the smartphone for everyone. In the development of some technologies, the power chip miniaturization also followed, but in order to consider voltage withstanding capacity, the microfilm processes also often encounter many difficulties. In the gate channel, the two hundred volts or more power devices currently require more than one micron channel length, but the overall device sizes are also up to twenty, thirty, or up to hundreds microns. In this paper, different types of silicon substrates are used to fabricate devices under the same processes [8,9] to make devices withstand the voltage above 200V, which are primarily used in a variety of motherboards.

The Difference Between Horizontal and Vertical Power Devices

There are two major directions for power devices development; one can withstand high voltages, and another can turn on a large amount of current. The power MOSFET among power devices with simple control circuits is fast and easy to operate in parallel. The different structures of power MOSFET can be divided into two broad categories: horizontal structure and vertical structure. Because the devices with horizontal structure can be integrated with CMOS, the power integrated circuit plays a very important role. As for devices with vertical structure can turn on a larger current and withstand greater voltage because of its vertical structure. However, it is difficult to integrate with integrated circuits of horizontal structure, so most are made of single discrete devices.

LDMOS

Lateral structure LDMOS increase the voltage withstanding by increasing the length of the drift region near the drain, so the wafer wastes a lot of space, and it will increase the on-resistance. Therefore, LDMOS constantly endeavors to reduce on-resistance, while still maintaining a very high voltage withstanding, as shown in Figure 1.

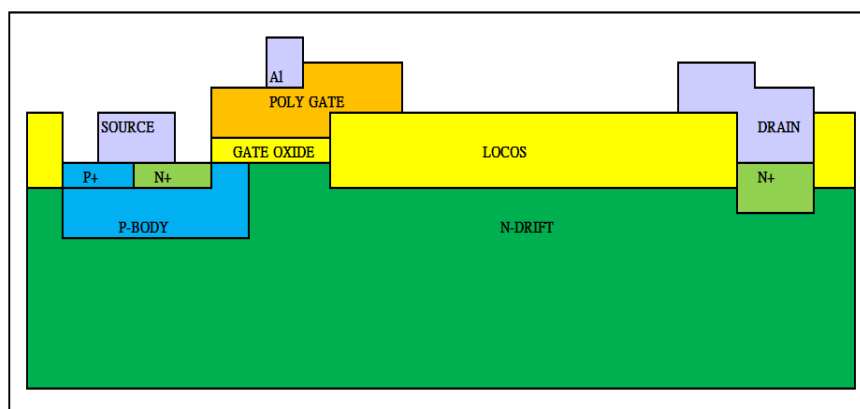


FIG. 1 LDMOS STRUCTURE DIAGRAM.

DMOSFET

Power MOSFET of vertical DMOS has several structures, and one of them is the V-MOSFET so named due to the gate of the V-shaped groove gate structure. This structure due to the unstable etching process may destabilize the starting voltage, and its V-shaped structure may result in a high degree of aggregation of the electric field to cause breakdown collapse. Therefore, V-MOSFET structures are replaced by DMOSFET.

Analysis and Discussion

Selection between the silicon wafer and the SOI substrate is currently still the main industry and academic research. However, in the voltage withstanding characteristic of these two substrates, the devices fabricated in the silicon wafer exists the electric potential underlying substrate itself when a voltage is applied. In the study of 200 V power devices, especially for the epitaxial layer thickness of the SOI substrate, devices with 1 micron of epitaxial layer can withstand the breakdown voltage up to 200 V; devices with 10 microns of epitaxial layer can withstand the breakdown voltage up to 300 V; however, the voltage withstanding of devices with more than 10 microns of epitaxial layer decreases. Simply, when the epitaxial layer thickness exceeds a certain level, the characteristics of the device itself is the same as that of the Bulk substrate. The relation of breakdown voltage and the epitaxial layer thickness can also be seen in Figure 2. In the analysis of the breakdown voltage, devices on the SOI substrate can withstand high voltage up to 210 V, as shown in Figure 5. However, devices on the silicon substrate can withstand high voltage only up to 208 V, as shown in Figure 6. There is no big characteristics difference between these two devices, but the driving current of devices on SOI substrate is smaller when operated at 5V, resulting in energy saving. In the electric field analysis, the field near electric gate region and drain regions of the SOI substrate is relatively uniform, and is also more stable compared with the devices on the silicon substrate, as shown in Figures 9 and 10. In the manufacturing, SOI substrate is a major market trend in the future.

Conclusions

In production of devices reaching 200 V breakdown voltages, the driving current of devices on SOI substrate is smaller than that of devices on Bulk silicon substrate, resulting in the reduction of power consumption. For the electric field uniformity, the device on SOI substrate is better than the device on Silicon substrate. As for voltage withstanding characteristics and operating characteristics, it can be seen from the analysis results that the characteristics of the SOI substrate are in superior to that of Bulk silicon substrate. In the future, when integrated with other devices, it will be able to effectively reduce the problem of power loss if SOI substrate is used in the production.

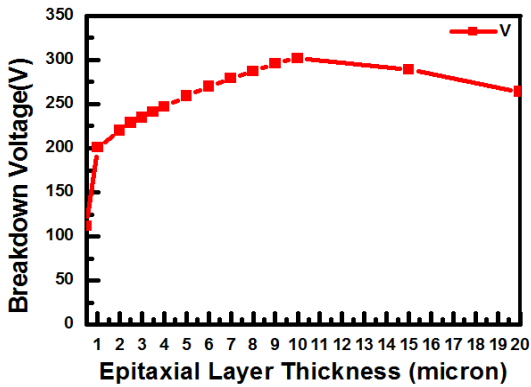


FIG. 2 200V LDMOS SOI STRUCTURE, EPITAXIAL LAYER THICKNESS AND THE RELATIONSHIP BETWEEN BREAKDOWN VOLTAGES.

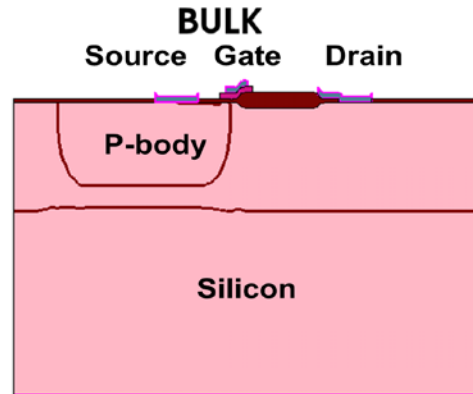


FIG. 3 200V POWER DEVICE SIMULATION OF BULK SILICON SUBSTRATE STRUCTURE.

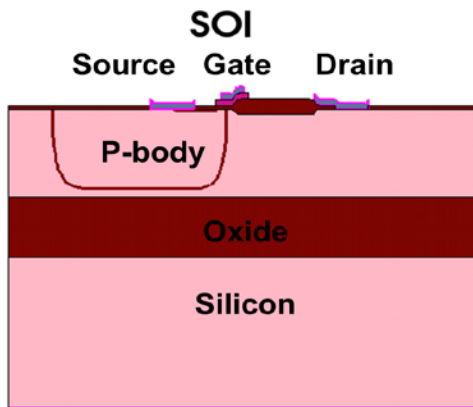


FIG. 4 200V POWER DEVICE SIMULATION OF SOI SILICON SUBSTRATE STRUCTURE.

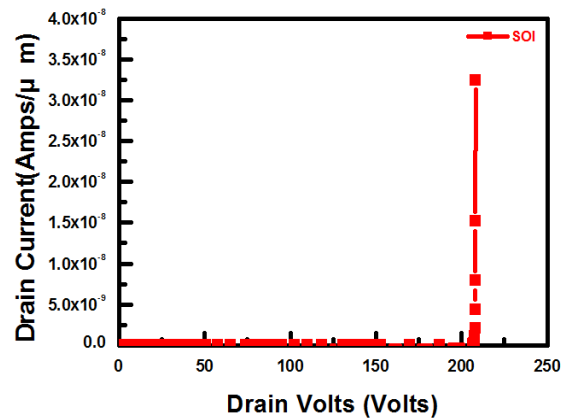


FIG. 5 SOI SUBSTRATES OFF-STATE BREAKDOWN VOLTAGES HAVE 210V.

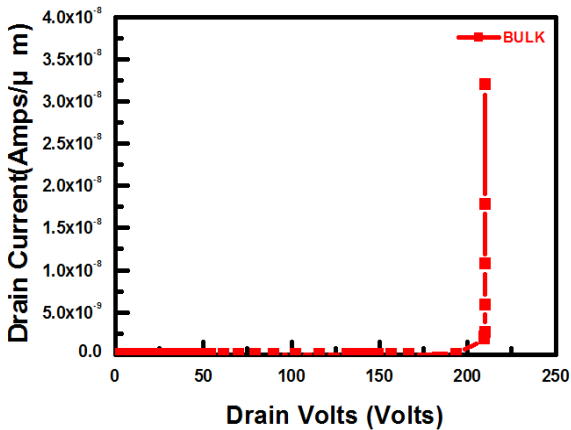


FIG. 6 BULK SUBSTRATES OFF-STATE BREAKDOWN VOLTAGES HAVE 208V.

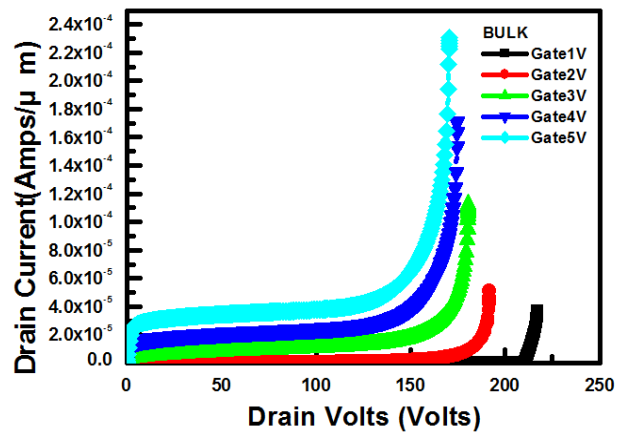


FIG. 7 BULK SUBSTRATES GIVE THE GATE VOLTAGE OF 1V ~ 5V, BULK SUBSTRATES ON-STATE BREAKDOWN VOLTAGES.

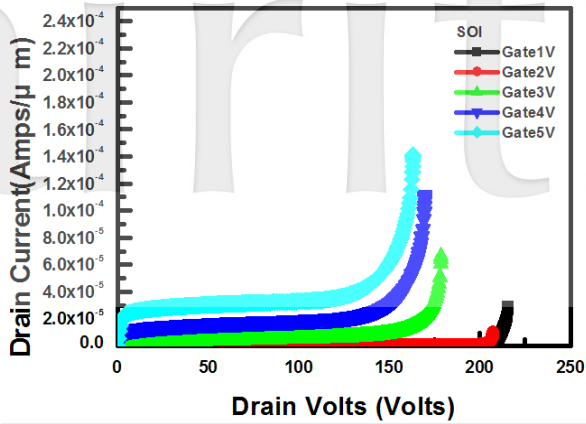


FIG. 8 SOI SUBSTRATES GIVE THE GATE VOLTAGE OF 1V ~ 5V, SOI SUBSTRATES ON-STATE BREAKDOWN VOLTAGES.

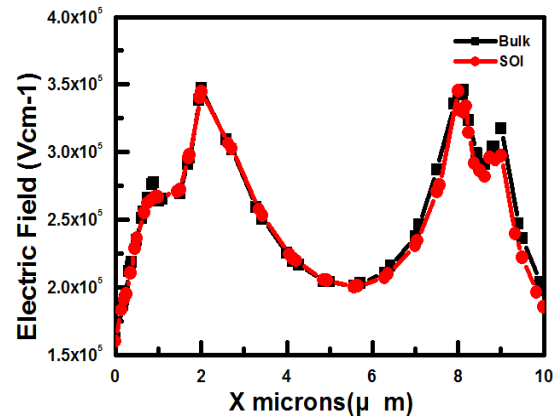


FIG. 9 ELECTRIC FIELD OF DIFFERENT SUBTRACTS FOR 1V

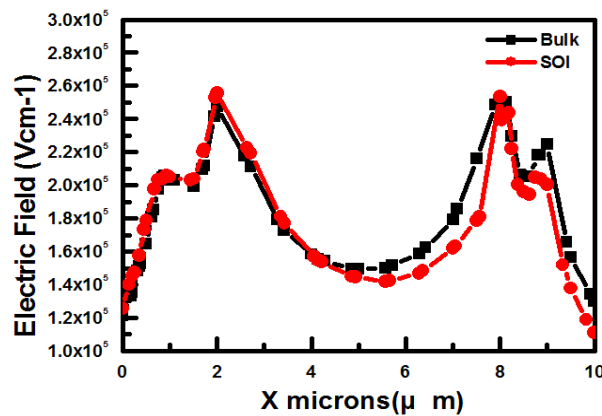


FIG. 10 ELECTRIC FIELD OF DIFFERENT SUBTRACTS FOR 5V

ACKNOWLEDGMENT

This paper thanks the assistance of National Science Council (MOST 103-2221-E-167-035), process parameter data of National Nano Device Laboratories as well as the assistance of National Center for High-Performance Computing to provide TCAD software.

REFERENCES

- [1] B. J. BALIGA, "Evolution of MOS-Bipolar Power Semiconductor Technology", PROCEEDINGS OF THE IEEE, VOL. 76, NO. 4, P.409, 1988
- [2] B. J. BALIGA, "Trends in Power Semiconductor Devices", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 43, NO. 10, P.1717, 1996
- [3] B. J. BALIGA, "The Future of Power Semiconductor Device Technology", PROCEEDINGS OF THE IEEE, VOL. 89, NO. 6, P.822, 2001
- [4] A. A. TAMER, K. RAUCH and J. L. MOLL, "Numerical Comparison of DMOS, VMOS, and UMOS Power Transistors", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-30, NO. 1, P. 73, 1983
- [5] C. N. Liao, F. T. Chien, C. W. Chen, C. H. Cheng and Y. T. Tsai, "High performance power VDMOSFETs with a split-gate floating np-well design", Semicond. Sci. Technol. VOL .23, P. 122001, 2008
- [6] H. Iwamoto, H. Haruguchi, Y. Tomomatsu, J. F. Donlon and E. R. Motto, "A New Punch-Through IGBT Having a New n-Buffer Layer", IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, VOL. 38, NO. 1, P. 168, 2002
- [7] B. J. Daniel, C. D. Parikh and M. B. Patil, "Modeling of the CoolMOS™ Transistor—Part I: Device Physics", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 49, NO. 5, P.916, 2002

- [8] S. K. Chung, "An Analytical Model for Breakdown Voltage of Surface Implanted SOI RESURF LDMOS", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 5, P. 1006, 2000
- [9] E. Napoli, "Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS", IEEE ELECTRON DEVICE LETTERS, VOL. 28, NO. 8, P. 753, 2007



Cheng-yen wu was born in Hsinchu, Taiwan,R.O.C., on May 7,1975. He received the master degrees in Computer Science and Information engineering from Asia University, Taichung,Taiwan, in 2009. He is currently pursuing the Ph.D. degree in the Ph.D. Program of Electrical and Communications Engineering at Feng Chia University. His research interests include semiconductor process and semiconductor simulation.



Hsin-Chiang You was born in Changhua, Taiwan,R.O.C., on May 23, 1977. He received the B.S.and M.S. degrees in electrical engineering from Feng Chia University, Taichung,Taiwan, in 1999 and 2001,respectively. He received the Ph.D. degree in electronics engineering from National Chiao-Tung University,Hsinchu, Taiwan, R.O.C., in 2006. His Ph.D. dissertation research focused on nano-devices and memories. From 2007 to 2009, he was with the Department of Computer Science and Information Engineering, Asia University,Taichung, Taiwan, as an Assistant Professor. In 2009, he joined the Department of Electronic Engineering,National Chin-Yi University of Technology, Taichung,Taiwan. R.O.C., and currently he is an Assistant Professor. His research interests include nano-devices and flexible

devices.



Chen-Chung Liu received the B.S. degree in applied mathematics from the National Chung-Hsing University, Taiwan, in 1976. He received M.S. degree in physical oceanography from the National Taiwan University, Taiwan, in 1980. He spent two years (1982/83) at the National Taiwan Natural Science Museum as an assistant researcher. At present he is a Professor and head of Department of Electronic Engineering at National Chin-Yi University of Technology, Taiwan. His research interests include computer graphics, pattern recognition, image analysis, and digital signal processing.



Wen-Luh Yang was born in Taichung, Taiwan, R.O.C, on May 5, 1961. He received the B.S. degree from the Department of Electrophysics, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1983, and the M.S. and Ph.D. degrees in Electronics from NCTU, in 1987 and 1992, respectively. In 1993, he joined the faculty of Feng Chia University (FCU), Taichung, as an associate professor with the Department of Electrical Engineering. From 2000 to 2004, he was the Professor and Chairman with the Department of Electronic Engineering. From 2004 to 2006, he was the Associate Dean with the College of Information and Electrical Engineering, the Chairman with the Honor Program of Information and Electrical Engineering, the Director with the Master Program of the Extended Education, and the Chief Executive Officer with the Master Program of Industrial R&D. Presently, Prof. Yang is a Professor with the Department of Electronic Engineering of FCU, an Advisor with the Department of Electronic Engineering of NCTC, an Evaluators with the Department of Electrical Engineering of National Chung Hsing University, and an Independent Director of the SOLID STATE SYSTEM CO., LTD (Flash Disk Innovators). His research interests include SONOS flash memory, ReRAM, FUSI and high-K dielectrics, strained Si, ultra shallow junctions, metal silicides, Cu and low-K dielectrics multi-level interconnections, nanoelectronics, and bioelectronics.